

**QUESTION #1****MARKS: 10 (2 + 2 + 2 + 2 + 2)**

Indicate (in the space provided) whether the following are TRUE or FALSE. Include a SHORT sentence in support of your answer. Do any FIVE (5).

Please note that each INCORRECT answer will be penalized 1 mark.

F-1) Device Well, diffusion, and thinox all refer to the same thing.

False ✓ 2) The 3 in CMOS3DLM refers to the minimum layout feature size.

The 3 means the actual minimum feature size is 3 μm

Min layout size is 3 μm

False ✓ 3) Circuits designed by the University of Saskatchewan are fabricated by the Canadian Microelectronics Corporation (CMC) in Kingston, Ontario.

They are fabricated by Northern Infratech (BNA) in Ottawa, Ontario.

True ✓ 4) Bipolar CMOS (BiCMOS) is the technology of the future.

This technology is currently being researched

Not future

False ✓ 5) Field oxide (FOX) exists everywhere that thin oxide (TOX) doesn't.

FOX can exist over top of TOX at the end of the process

WHY? in manufacturing

FOX and TOX don't exist in one

This performs a standard NAND function

True ✓ 6) The Metal2-Via enclosure rule is larger than the Metal1-Contact enclosure rule.

The Metal2-Via enclosure rule is 3 μm  
and the Metal1-Contact enclosure rule is 2 μm

Name: \_\_\_\_\_

- 2 -

Student Number: \_\_\_\_\_

Name: \_\_\_\_\_

- 3 -

Student Number: \_\_\_\_\_

"The reason why we have midterms is not because we're not allowed to extract  
your fingernails with a pincer."

**QUESTION #2****MARKS: 15 (5 + 10)**

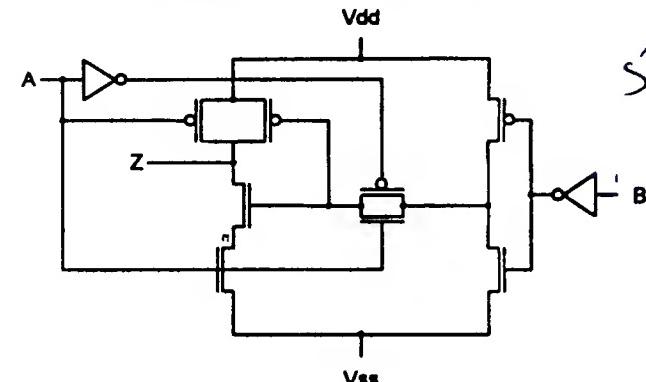
- a) The circuit shown in the figure below is a logic gate. Determine the logical purpose. What standard logic gate does it implement?



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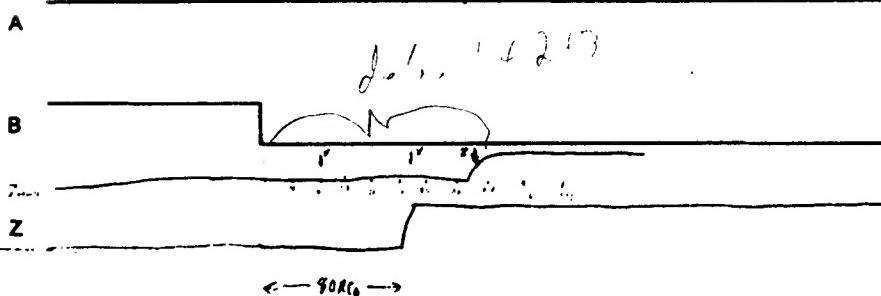
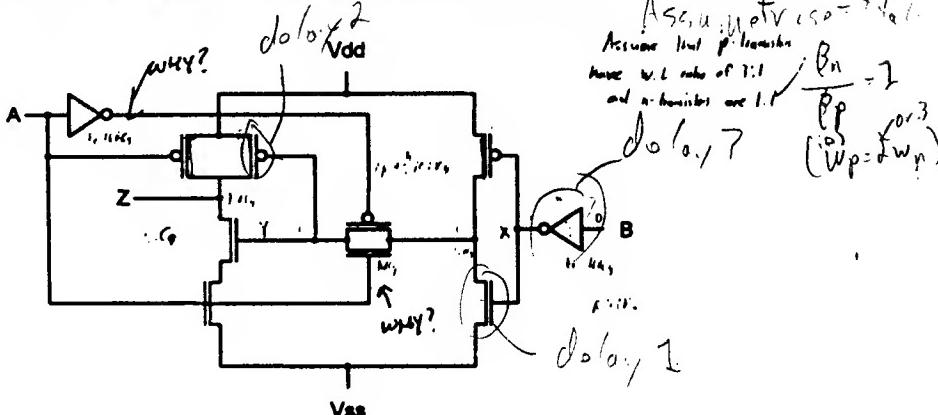
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A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0



- b) The circuit schematic from Part a) is shown below. For the input waveforms shown, what is the approximate delay time from the B input going low (Vdd volts to Vss volts, 2ns fall time) and the Z output changing level?

State any assumptions that you make. All assumptions must be valid and have some basis in fact.



Assumptions:  
All gate numbers to MSI  
M1, M2, Transistor 2  
Switching off by 100  
Analog  
Analog is then not necessary  
Digital is adjusted to

How? 5  
 Delay 1 is 1/(4L<sub>1</sub>) = 80RG  
 Delay 2 is 3/(3L<sub>1</sub>+2L<sub>2</sub>) = 1.8RG  
 Delay 3 is 2/(2L<sub>1</sub>) = 1.6RG  
 Total is 1.8RG + 1.6RG = 3.4RG  
 Total is 3.4RG + 1.8RG = 5.2RG  
 Total is 5.2RG + 1.6RG = 6.8RG  
 Total is 6.8RG + 1.6RG = 8.4RG  
 Total is 8.4RG + 1.6RG = 10.0RG

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Student Number: \_\_\_\_\_

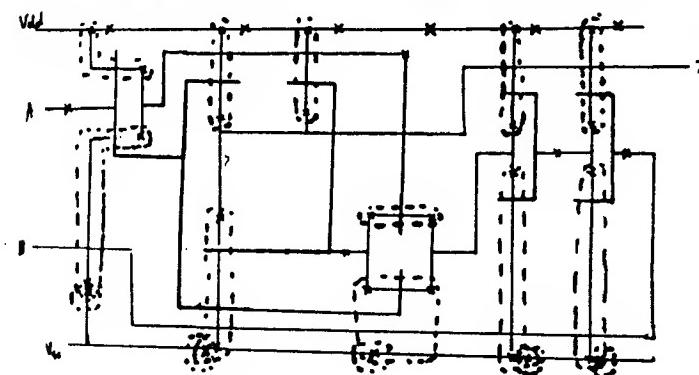
## QUESTION #3

MARKS: 20 (20)

- a) From the circuit schematic shown in Question #2 Parts a) and b) draw a STICKS diagram for the circuit.

You must use the following constraints in drawing your STICKS diagram:

- Use E.E. 451.3 standard STICK colors and patterns.
- Show p+ and P-well. Do not show p-guard or N-well.
- A and B must come in from the same side. Z must leave from the other side. Label the input and output lines.
- No interconnection layers are allowed to lie outside the Vdd and Vss power supply rails.
- At least one (1) Vdd substrate contact and one (1) Vss substrate contact must be shown.



20

Name: \_\_\_\_\_

-5-

Student Number: \_\_\_\_\_

"No, no, no... let me ask someone who doesn't know so I can scream at them."

**MARKS: 10 (10)**

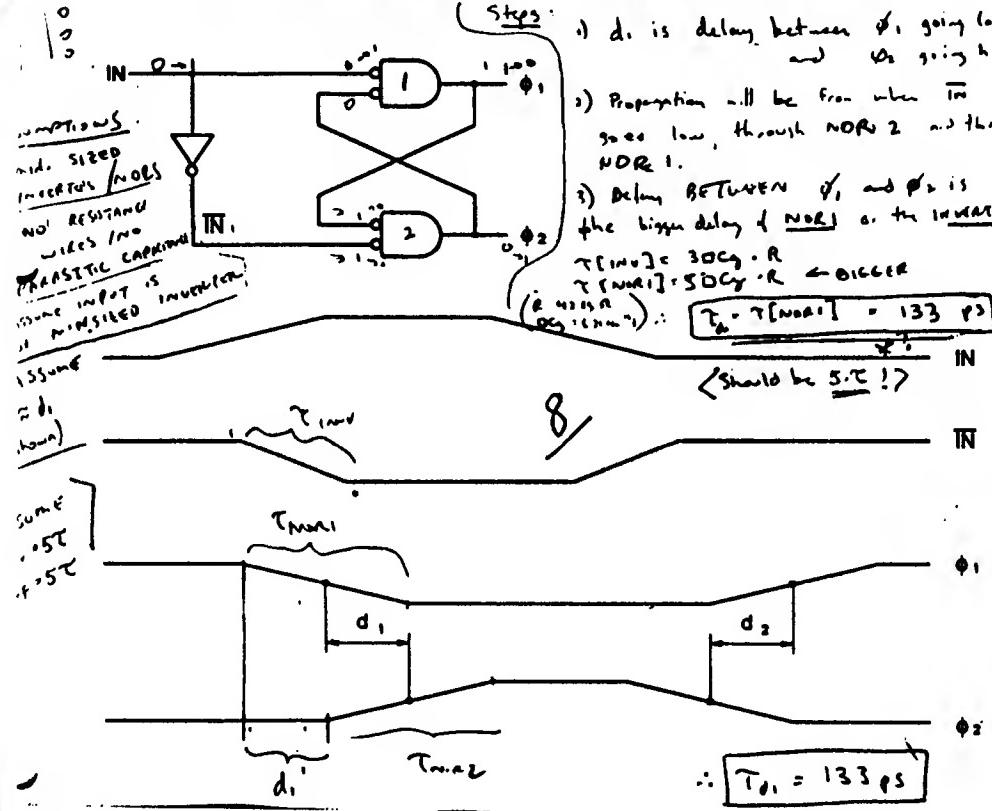
— 1 —

The following circuit serves a useful purpose. It was discussed in class.

- a) Determine the dead zone time ( $d_1$  or  $d_2$ , pick either one, your choice). Representative waveforms are shown below.

State any assumption(s) that you make. I might suggest two (2) that will make your task easier:

- 1) Assume linear rise and fall times, even though you may be using exponential waveforms.
  - 2) Assume constant pull-up and/or pull-down resistance during transitions.



(about midterm marks) "I have to use the Wonder-Bra method: push it up as much as you can!"

**MARKS: 15 (3 + 3 + 3 + 3 + 3)**

Explain briefly, but as completely as possible, FIVE (5) of the following. A SHORT paragraph should be sufficient.

- a) Design rule E.1 concerns the overlap of Poly over Device Well (see Appendix C: Available Process Technologies, page C9). It is given as 5 design scale microns (dsm). What is the basis for this rule?

If poly does not completely overlap the diffusion, there may be a short between Dicm and Source:



$$5 = -1$$

- b) Using CMOS technology complicates the fabrication process (with respect to nMOS). Give TWO (2) advantages of CMOS (with respect to nMOS). Give ONE (1) disadvantage of CMOS (with respect to nMOS).

## ADVANTAGES of $C_n$ 's:

- 1) Rise and fall times are of the same order.
  - 2) Almost zero static power dissipation.

(re rise times  
longer than fall)  
for  $\omega$  M/S

DISADVANTAGE.

- c) i) Requires  $2N$  devices for  $N$  inputs  
 (vs  $N+1$  devices for  $N$  AOS)

CMC located at Queen's University in Kingston, Ontario,  
by Northern Telecom located in Ottawa, Ontario.

- d) Technically speaking, is the circuit shown in Question #1 of this examination paper level-activated or edge-triggered? Is it a latch or a flip-flop? Explain.

- LEVEL ACTIVATED, OUTPUT CHANGES ON BOTH EDGES  
TICKETED IT IS NOT EDGE ACTIVATED

- NO memory, i.e. NOT A FLIP FLOP

- OUTPUT follows INPUT (Complementary), i.e. LATCH

- e) List THREE (3) ELECTRIC™ keyboard commands that you have used. Give a SHORT description of each one.

- 1) -help(x) will show a short description of command x, if one is available
- 2) -tellid simulation(x) Selects ELECTRIC to prepare a simulation for x (x is usually esim or spice)
- 3) -onaid simulation : Tells ELECTRIC to begin simulation preparation for the package specified in "tellid simulation(x)"

- f) What is the essential difference between Gate Array design and Field Programmable Gate Array design? Which one is "better" (define "better" in your answer)?

Gate Array: Can only be "mask-programmed": I.E., "Programmed" AT THE FABRICATION SITE, BY FABRICATORS.

FPGAs: CAN BE "FIELD" PROGRAMMED BY THE DESIGNERS. (AT THE DESIGN SITE).

FPGAs are BETTER, if BETTER means quicker turnaround time, cheaper and easier to debug designs.

"This means that everyone who was alive and halfway breathing and not thinking about sex got it right."

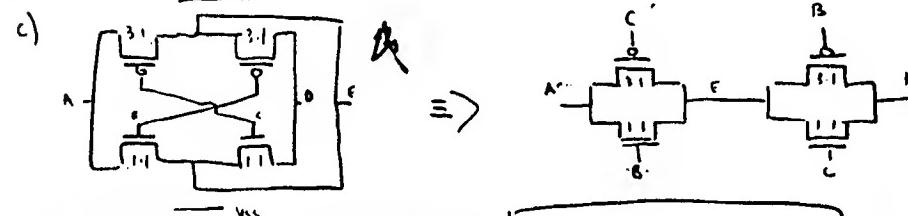
## QUESTION #3

MARKS: 20 (8 + 3 + 4 + 5)

It is desirable for VLSI designers to "reverse engineer" circuits that have been created by other VLSI designers. In this way you can see other ways of doing the "obvious" and thereby learn new techniques that can be used in circumstances that may arise in your personal integrated circuit designs, such as on examinations.

- a) Shown on the next page is a standard cell for a useful logic design function. From the Laser\_plot plot of the cell determine the STICKS diagram for the circuit. This may be done by "coloring" the Laser\_plot. Where appropriate, "Coloring" may consist of a single line down the center of each layer polygon that is visible. Make sure that you use EE 451.3 standard colors.
- b) How many split-contact cuts are there in the Laser\_plot? Normal contact cuts? Vias?
- c) From the STICKS diagram determine the circuit schematic (i.e., the transistor layout and interconnection) for the circuit. Make sure you show the transistor sizes in the circuit schematic (use W:L). Label the inputs and outputs.
- d) From the circuit schematic determine the truth-table for the circuit. Note potential problems with this circuit (if any).

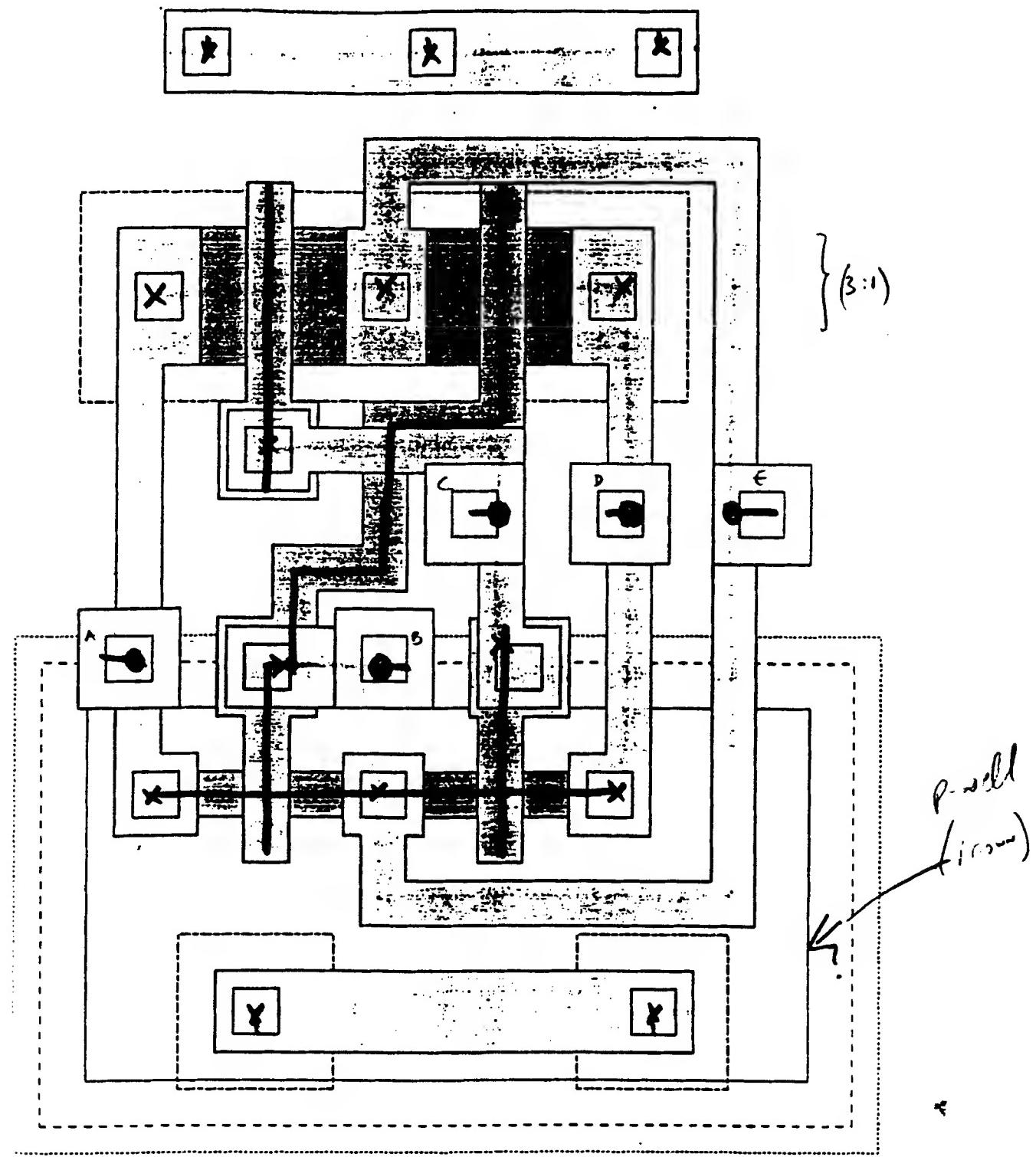
b) There are NO (zero) split contacts.  
There are FOURTEEN / contact cuts  
There are FIVE / vias



ASSUME: TRUTH TABLE VALUES GIVEN AT STEADY STATE				
A	B	C	D	E
0	0	0	0	0
0	0	1	E	A'
0	1	0	E'	A
0	1	1	0	0
1	0	0	1	1
1	0	1	E	A'
1	1	0	E'	A
1	1	1	1	1

INPUTS: A  
"2<sup>nd</sup> CLOCK" INPUTS: B, C  
OUTPUTS: E, D

Potential Problems:  
1) If B and C are NOT complementary then the circuit will propagate different values at different speeds (i.e.: for B=0 or B=C) to E.  
2) If B and C overlap on low or off, signal A will propagate through to D (transparent)

Laser\_plot

— = metal 2